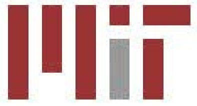

Anomalous Source-side Degradation of InAlN/GaN HEMTs under ON-state Stress

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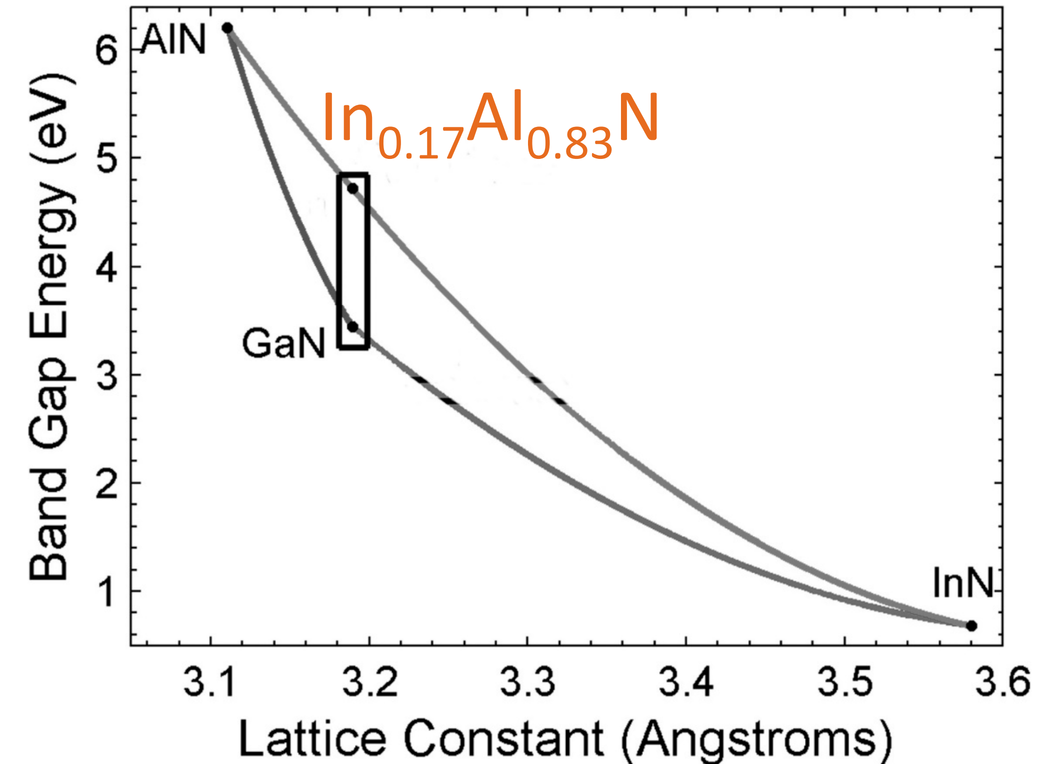
Outline

1. Motivation
2. Source-side degradation under ON-stress
3. Gate leakage current and its temperature dependence
4. Positive gate stress
5. Conclusions

Motivation: InAlN as barrier

	$Al_{0.2}Ga_{0.8}N/GaN$	$In_{0.17}Al_{0.83}N/GaN$
ΔP_0 ($e \cdot cm^{-2}$)	6.5×10^{12}	2.7×10^{13}
P_{piezo} ($e \cdot cm^{-2}$)	5.3×10^{12}	0
P_{total} ($e \cdot cm^{-2}$)	1.2×10^{13}	2.7×10^{13}

[J. Kuzmik, EDL 2001]



[M. A. Laurent, JAP 2014]

- High spontaneous polarization in InAlN → high 2DEG density
- InAlN thickness scaling → gate length scaling → W- and V-band applications

$In_{0.17}Al_{0.83}N$ lattice matched to GaN → Potentially better reliability!

Motivation: InAlN as barrier

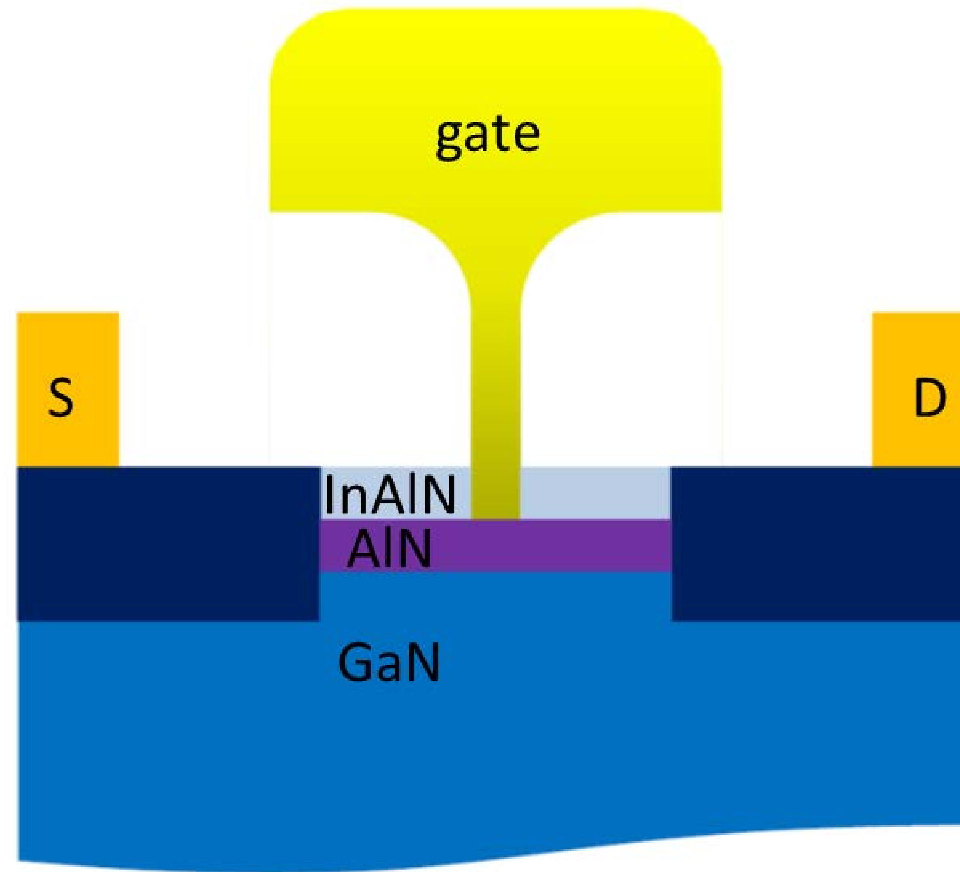
InAlN/GaN HEMTs

- W-band
- E-mode

Four gate geometries:

- W_g = 8 X 25 µm
- W_g = 8 X 50 µm
- W_g = 2 X 25 µm
- W_g = 2 X 50 µm

Thermal models available

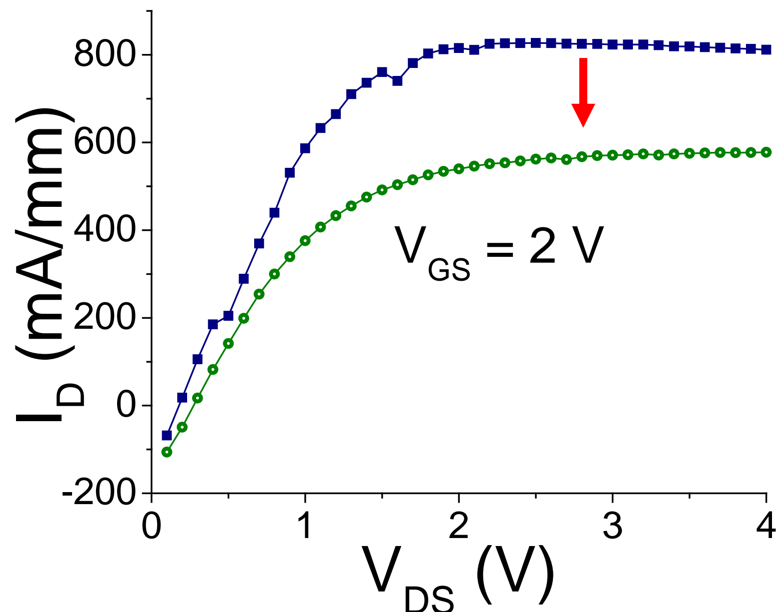


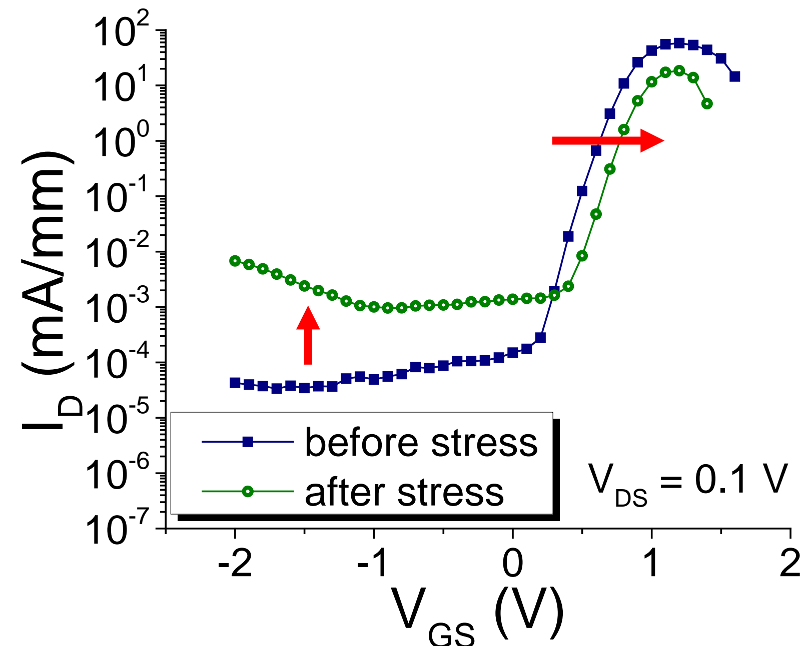
[Saunier, CSICS 2014]

High-V_{DS}-high-I_D stress

Stress and characterization conditions:

- $V_{DS,stress}$ = 25 V, $I_{Dstress}$ = 400 mA/mm (V_G ~ 1.5 V), 5 mins, RT (T_j ~ 136 °C)
- Characterization: @ 25 °C after thermal detrapping



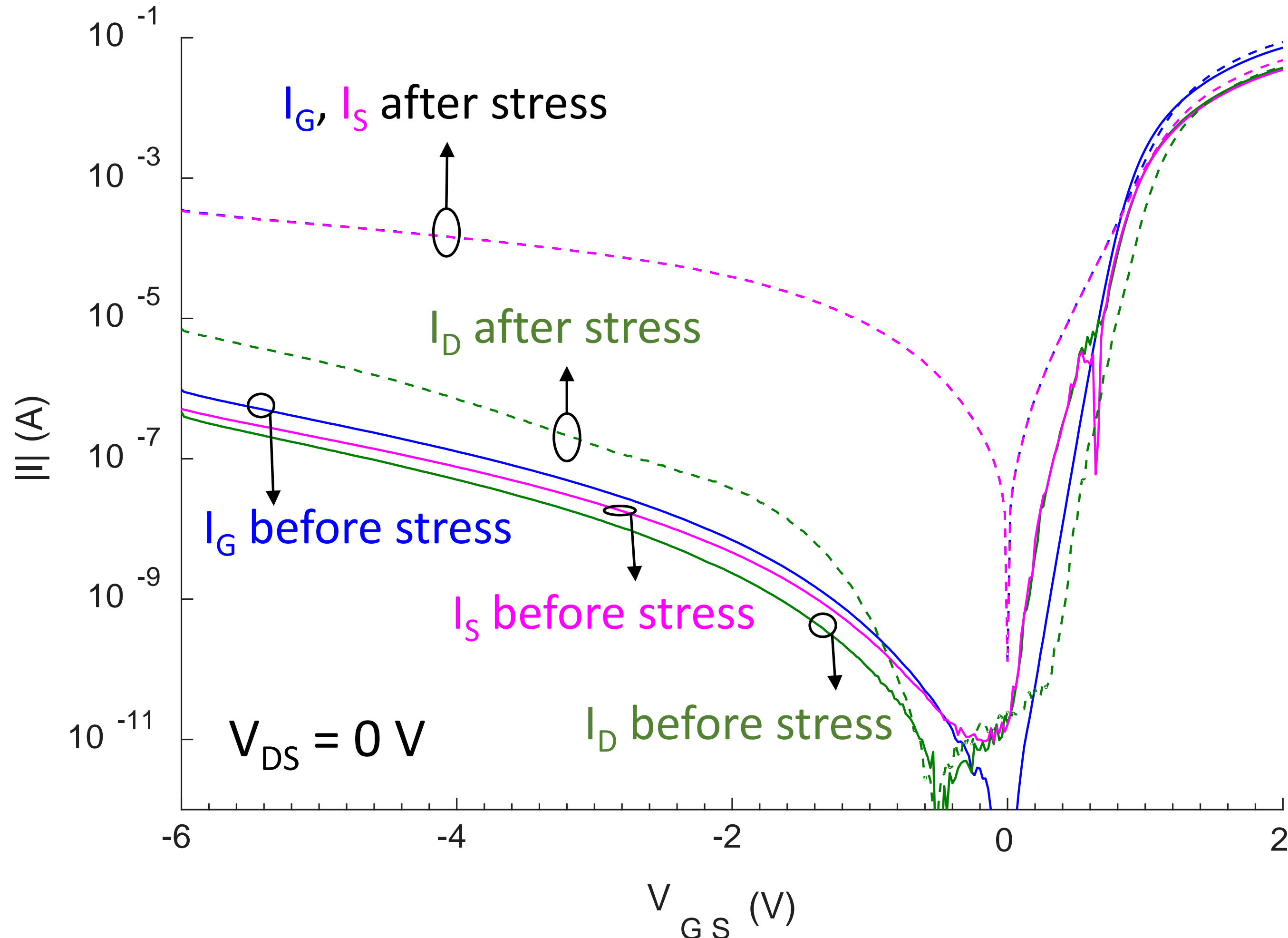


Permanent degradation:

- Significant I_{Dmax} degradation
- $\Delta V_T > 0$
- Significant I_{Doff} degradation

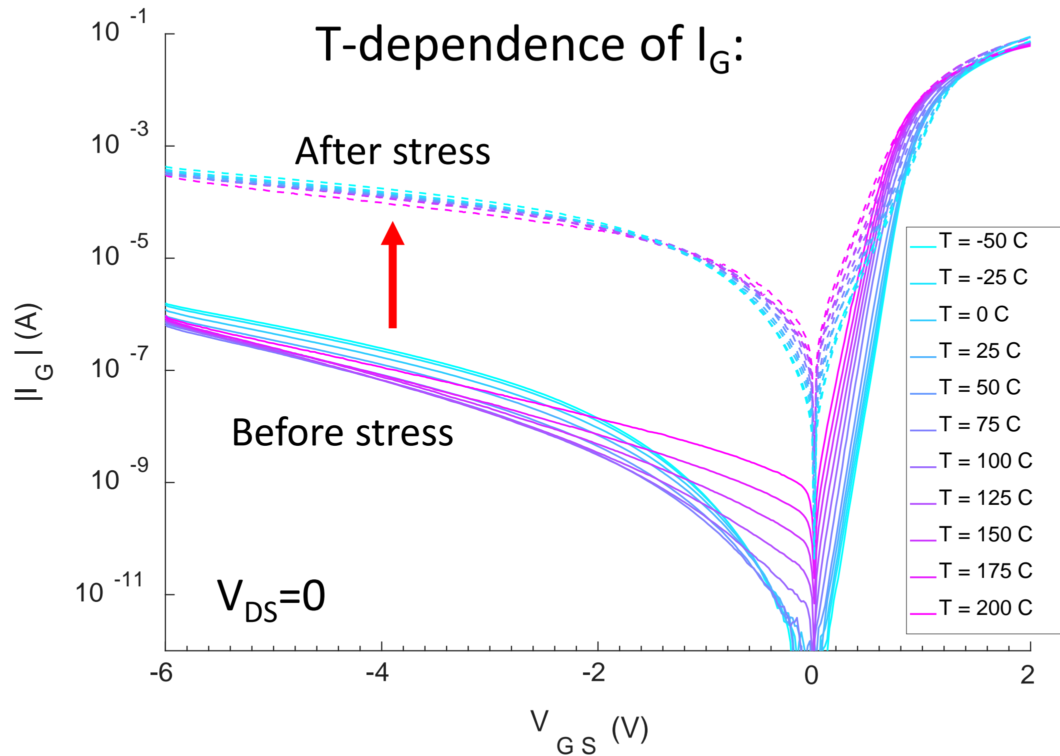
High-V_D-high-I_D stress

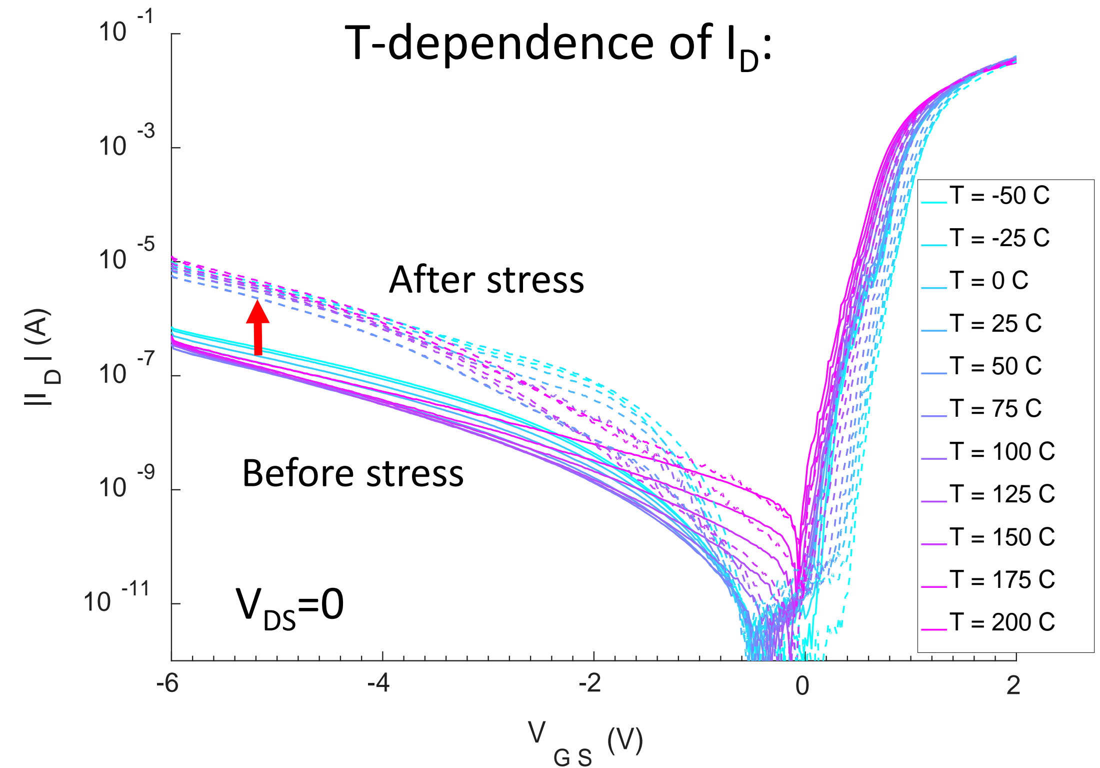
After thermal detrapping, gate current degradation:



- Large increase in I_G after stress
- After stress: $I_G = I_S >> I_D$ in forward and reverse bias
- **Source-side damage unexpected!**
- Uncommon but previously observed in AlGaN/GaN HEMTs [J. Joh, IEDM 2010]

Temperature dependence of I_G and I_D





Before stress:

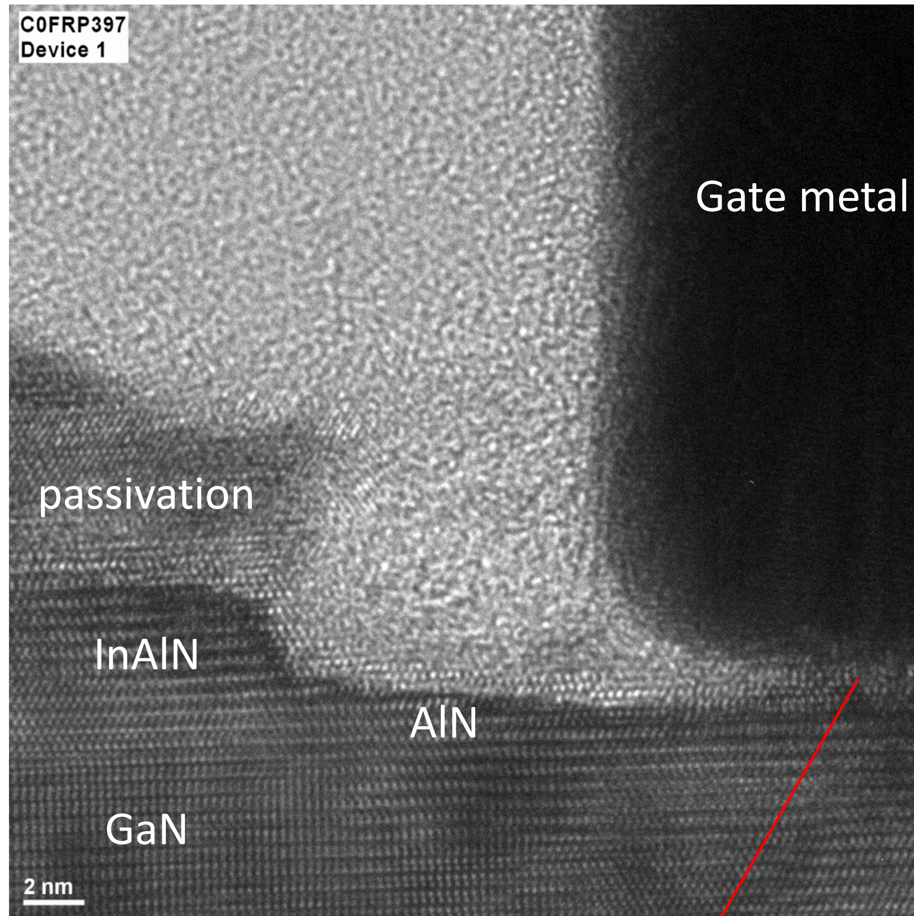
- For moderate V_{GS}, negative T coefficient → thermionic emission limited current
- I_S behaves similar to I_G

After stress:

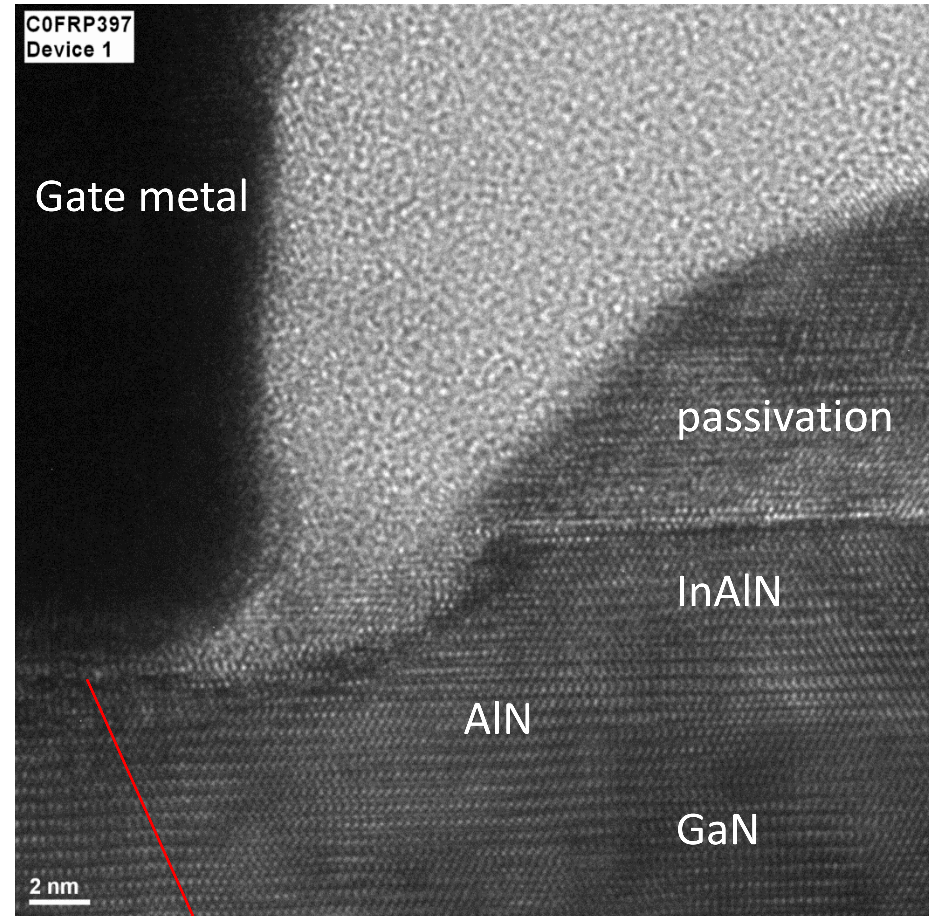
- Significantly reduced T dependence for I_G and I_S
- I_D less affected → degradation on source side

HRTEM of a virgin device

Virgin device drain side



Virgin device source side

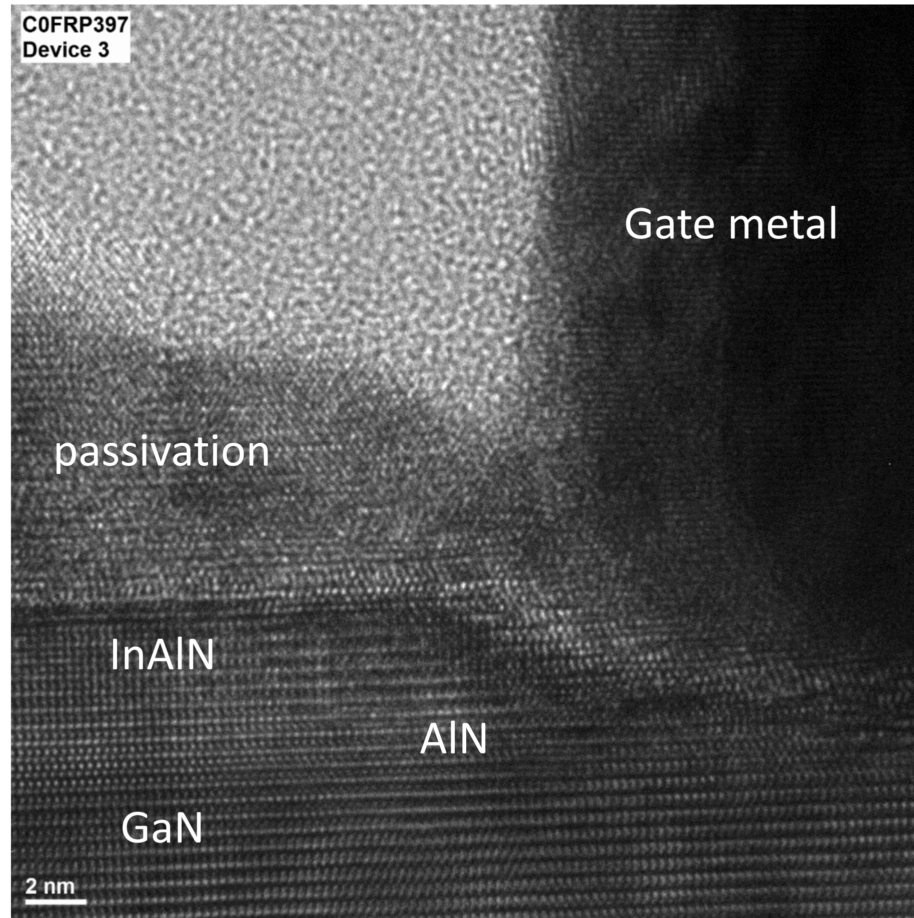


Residual oxide?

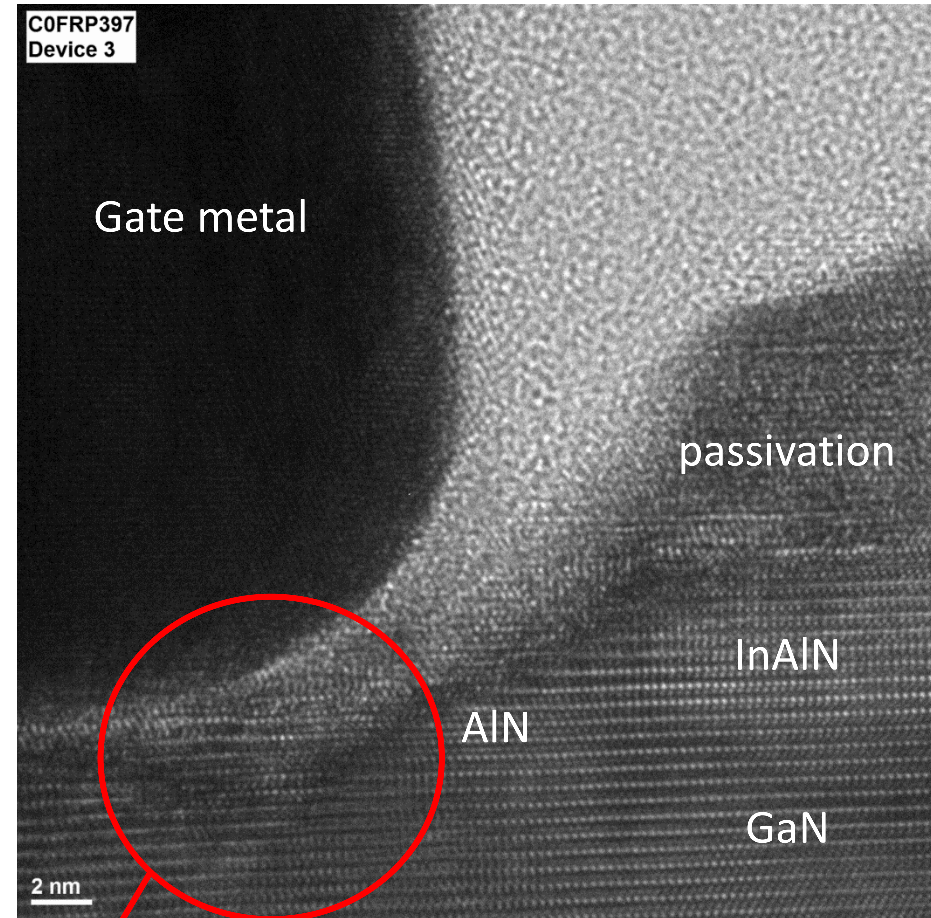
Gate recessed to the AlN interlayer

HRTEM of stressed device

Stressed device drain side



Stressed device source side



Disordered region in GaN channel at gate edge on source side

Hypothesis for Damage

High $V_{DS,stress}$ + high $I_{Dstress}$ → high $I_{Gstress}$ too

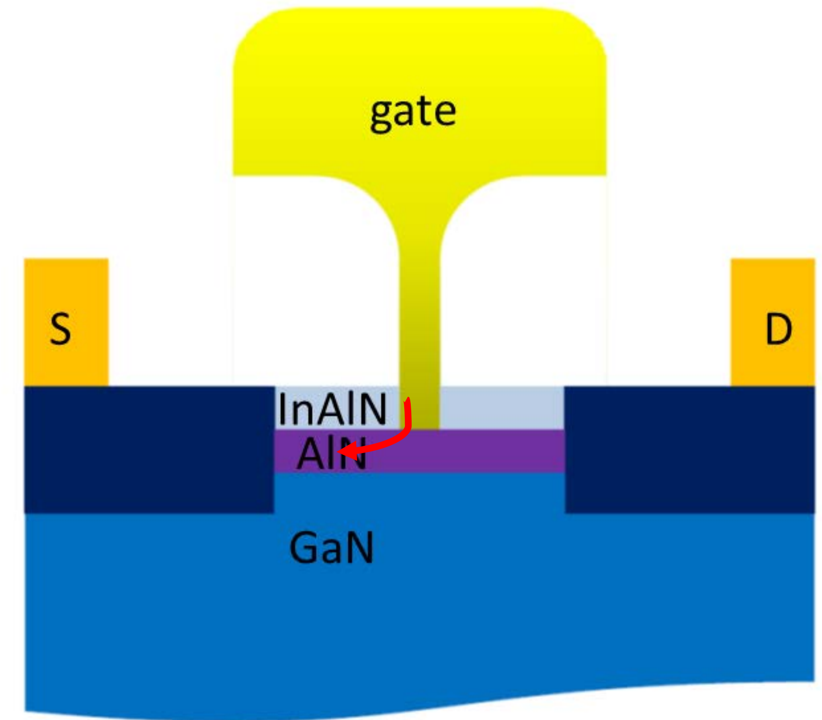
→ high I_{GS}

→ high T_j

→ high electric field across AlN barrier on source side

Conditions favor defect formation in AlN barrier on source side → I_{GS}↑

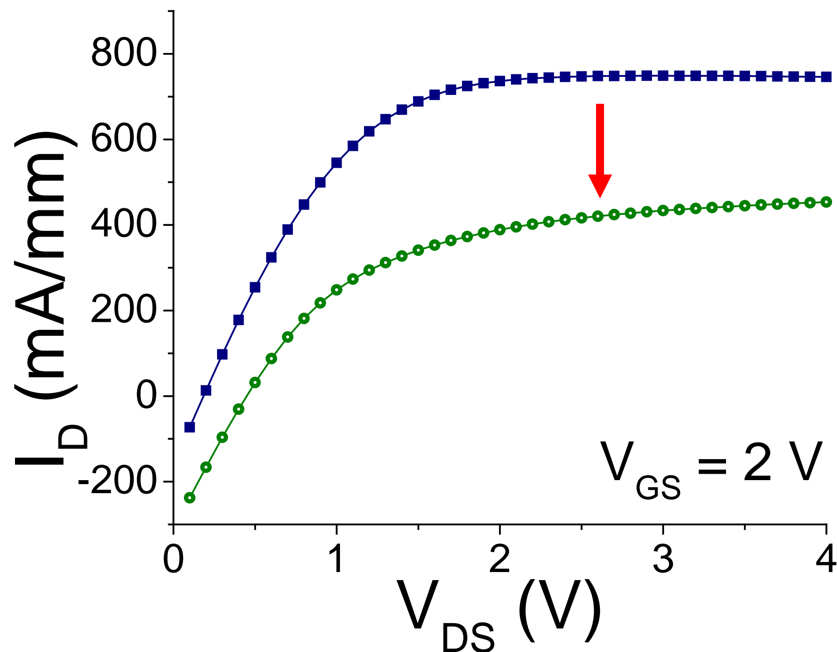
Also, gate sinking → $\Delta V_T > 0$

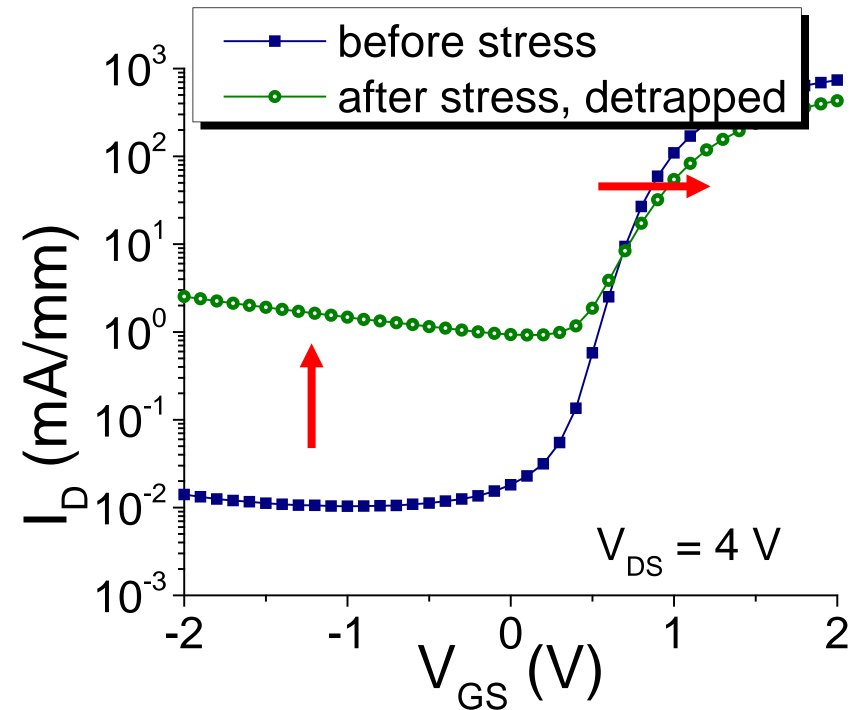


Positive V_G step-stress-recovery experiment

Stress and characterization conditions:

- $V_{GS,stress}$ = 0 - 2.5 V, $V_{DS,stress}$ = 0 V, step = 0.1 V, RT (T_j ~ 48 °C)
- Characterization: @ 25 °C after thermal detrapping





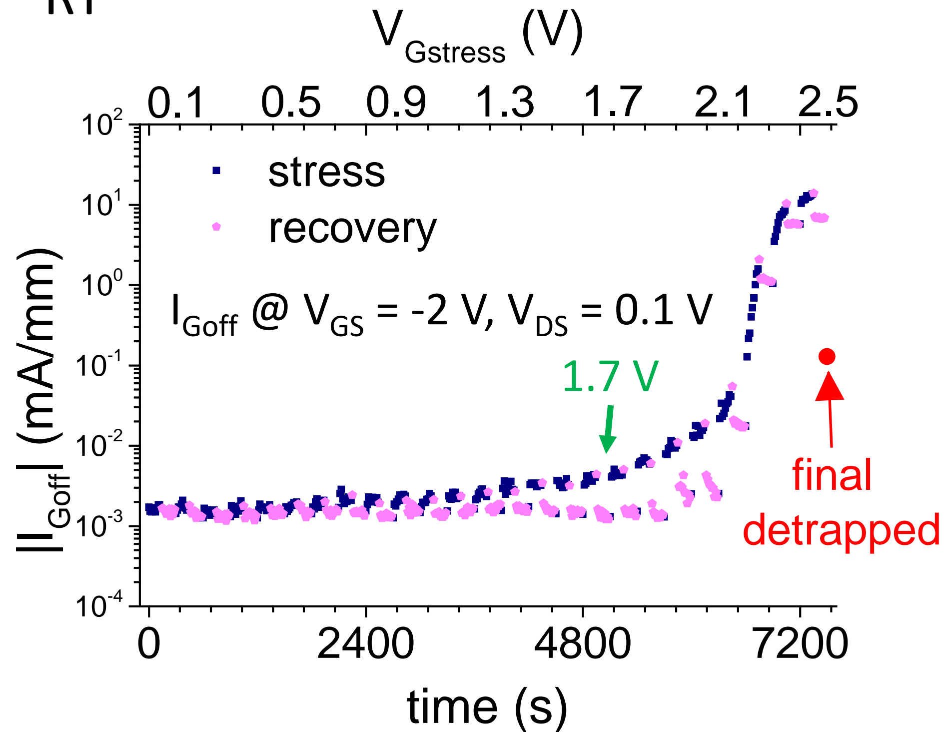
Permanent degradation:

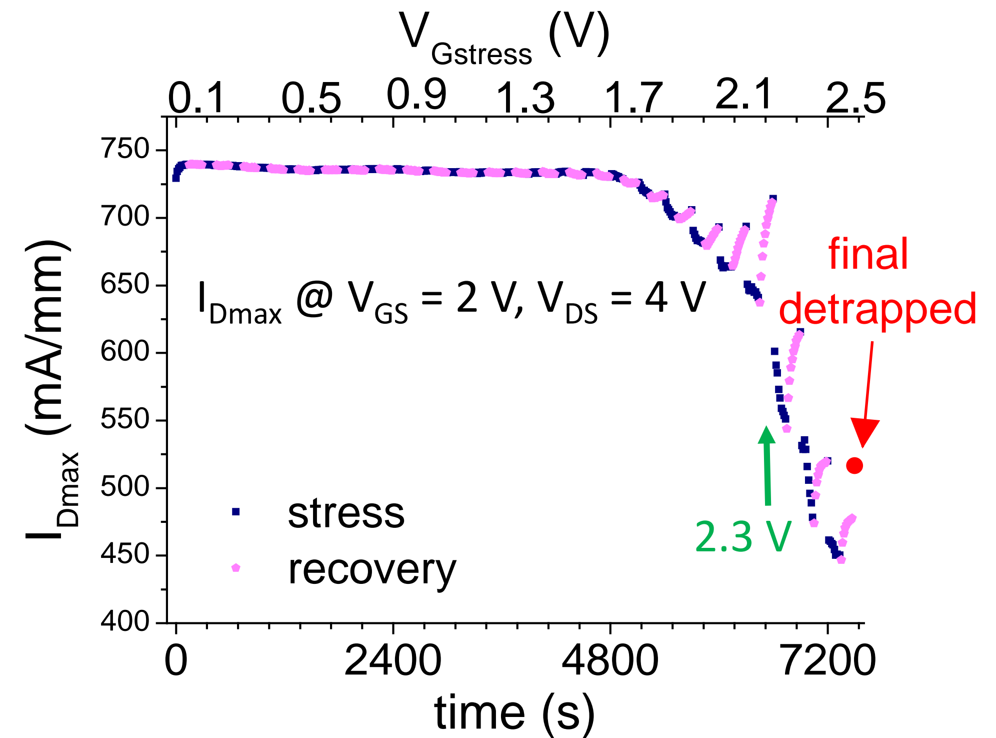
- Significant I_{Dmax} degradation
- $\Delta V_T > 0$
- Significant I_{Doff} degradation

Time evolution of I_{Dmax} and I_{Goff}

Stress conditions:

- $V_{DS,stress}$ = 0 V, $V_{GS,stress}$ = 0.1 – 2.5 V in 0.1 V steps
- stress time = recovery time = 150 s; characterization every 15 s
- RT



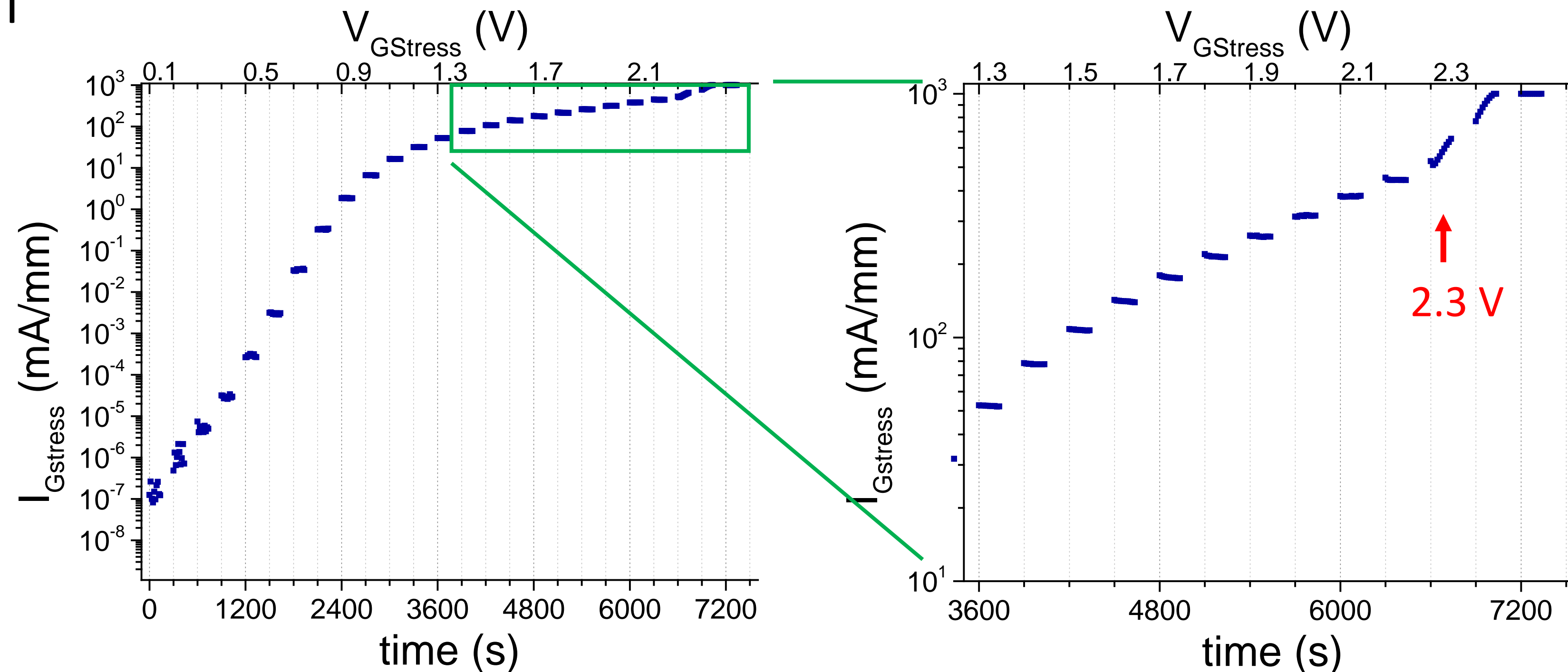


- $|I_{Goff}|$ starts to increase from $V_{GS,stress}$ ~ 1.7 V → trap generation in AlN
- I_{Dmax} starts to severely degrade from $V_{GS,stress}$ ~ 2.3 V → gate sinking

Time evolution of $I_{Gstress}$

Stress conditions:

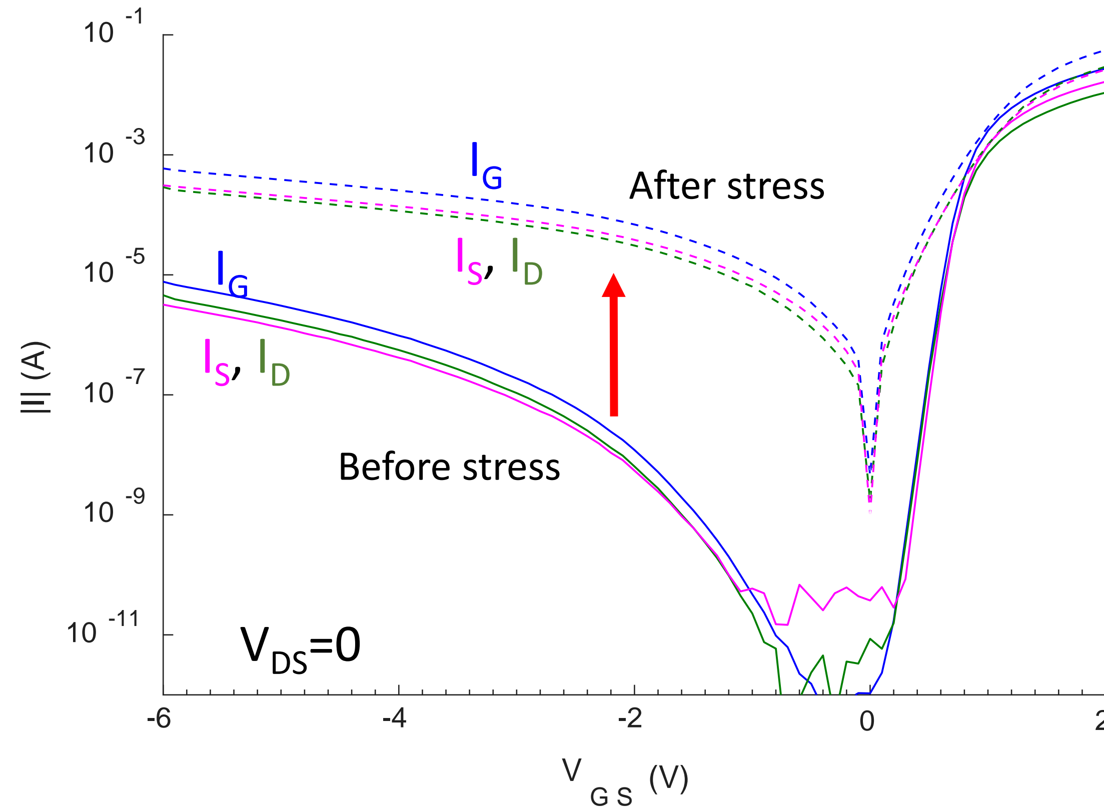
- $V_{DS,stress}$ = 0 V, $V_{GS,stress}$ = 0.1 – 2.5 V in 0.1 V steps
- stress time = recovery time = 150 s; characterization every 15 s
- RT



- $I_{Gstress}$ increase becomes significant for $V_{GS,stress}$ ≥ 2.3 V

Gate current degradation

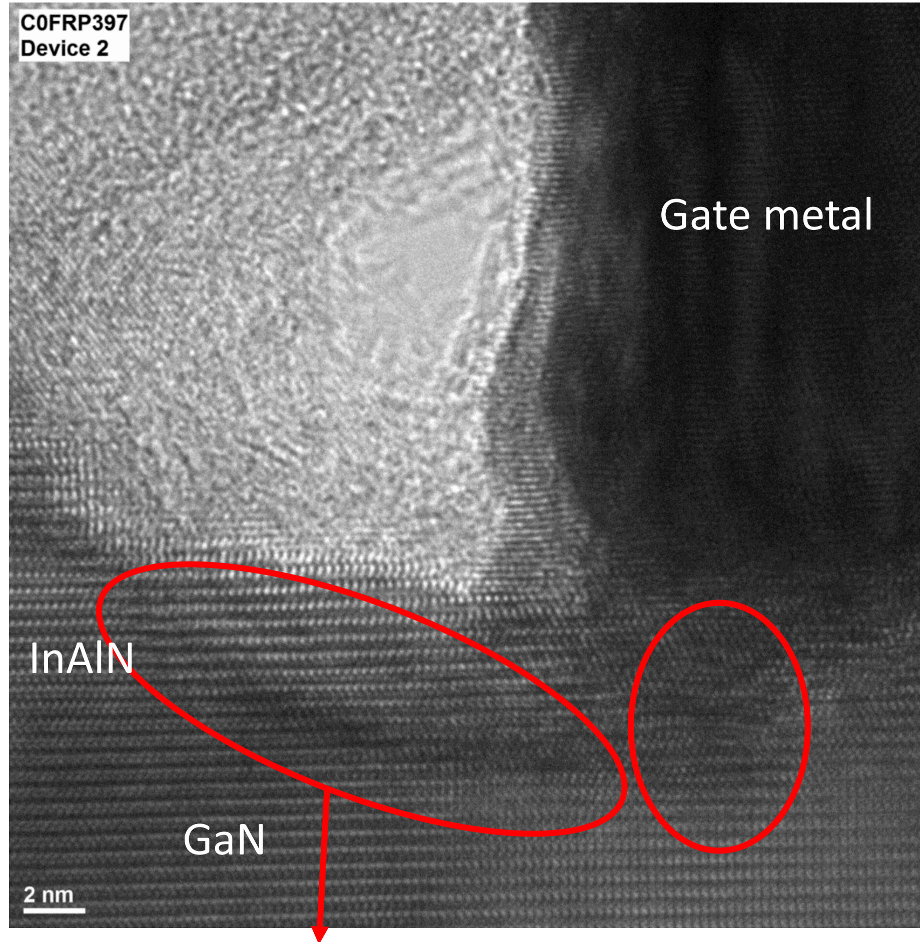
After thermal detrapping, gate current degradation:



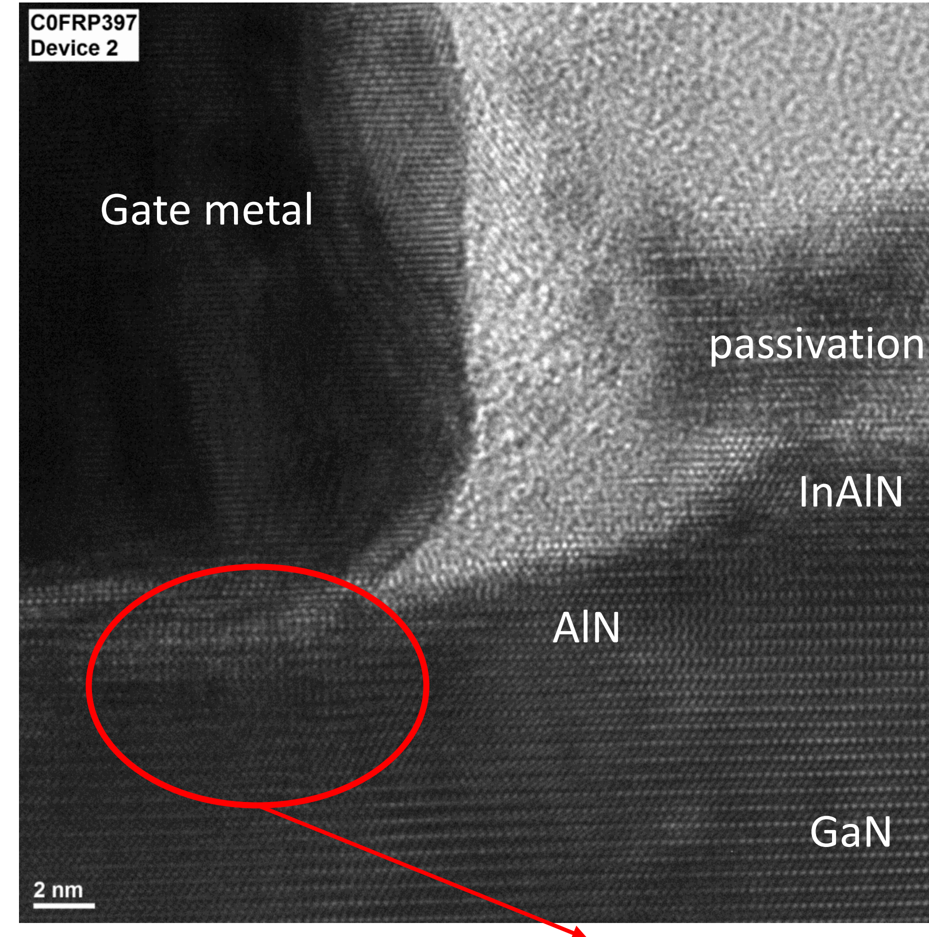
- Symmetric degradation: $I_S \approx I_D \approx I_G/2$
- Reproduced degradation signature of high-V_{DS}-high-I_D stress:
  high forward V_G leads to increase in I_G

HRTEM of stressed device

Stressed device drain side



Stressed device source side



Disordered region in GaN channel at gate edge on drain side

Disordered region in GaN channel at gate edge on source side

Conclusions

- Permanent degradation after High-V_{DS}-high-I_D stress:
  - I_{Goff} ↑↑ → Defect formation in AlN barrier on source side
  - $\Delta V_T > 0$, I_{Dmax} ↓↓ → Gate sinking
  - Affects source side

- Positive gate stress:
  - Reproduced degradation signature of high-V_{DS}-high-I_D stress:
    I_{Goff} ↑↑ , $\Delta V_T > 0$, I_{Dmax} ↓↓
  - $I_S \sim I_D \sim I_G/2$ → Symmetric degradation on source and drain side

Thank you
&
Questions?